ISSN: 2320-1363

A NEW H-BRIDGE INVERTER TOPOLOGY FOR ENHANCED EFFICIENT MULTILEVEL OPERATION

Mohd Samdani[1], M.M.Irfan[2], T.Ashok Kumar[3]
[1]M.Tech (PE) Student, Dept of EEE, SR Engineering College, Warangal AP, India
[2]Assistant Professor, Dept of EEE, SR Engineering College. Warangal AP, India
[3]Assistant Professor, Dept of EEE, SR Engineering College. Warangal AP, India

Abstract

In this paper mainly focused on the design and implementation of new topology based on H-bridge structure with four switches connected to the dc-link. Based on a POD (Phase opposition disposition) modulation method, a new PWM method which requires only one carrier signal is suggested. The switching sequence to balance the capacitor voltage is also considered. In addition to these, the proposed topology requires minimum number of component count to increase the number of voltage level. The main objective of this dissertation is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main merit of the new topology is to reduce the lower total harmonic distortion. In this dissertation, various carrier pulse width modulation techniques are proposed, which can minimize the total harmonic distortion and enhances the output voltages from proposed work of five-level inverter. The various switching topologies of single-phase five level cascaded H-bridge multilevel inverters have been analyzed in this dissertation. It is justified that the new topology can be recommended to single phase five level Cascaded H-bridge inverter for better performance in comparison with conventional method. The simulation is done by Mat Lab 10.0 version software

Keywords: POD, Cascaded Topologies, H- Bridge, SPWM

1. Introduction

The increasing demand for electrical energy, depleting fossil energy reserves and the increase in energy prices have necessitated to use the current energy resources more efficiently. Power electronic converters as the essential equipments to convert and control of electrical power in the wide range of mill watts to gig watts with the help of semiconductor devices are finding increased attention. Hence, highly efficient power electronic technologies and reliable control strategies are needed to reduce the waste of It is developed a general model for analyzing a variable speed drive with a multilevel inverter with the objective to verify the response of two control methods. Simulation models for multilevel inverter, induction machine and both control techniques are developed. A multilevel inverter and an induction machine have been used as prototypes. The design of the controllers has shown that the whole performance of the two control schemes is comparable. In this paper, POD (phase opposition and

ISSN: 2320-1363

disposition) technique has been implemented for a Multilevel Inverter with D.C link switches. Compared to the conventional SPWM techniques used for inverter operation , POD technique when applied to the above stated topology is advantageous since the main H-Bridge switches are switched at fundamental output voltage frequency unlike the in case of SPWM where they are switched at frequency equal to High frequency triangular wave. Tehre by switching losses in this topology are restricted to minimum possible levels. For the purpose of comparison simulations are carried out for energy and to improve power quality. One of the most significant potentials to improve the efficiency of electrical energy in industry is electric motor drive systems.

High power inverters and medium voltage drives have been studied intensively since the mid-1980s for industrial applications. These inverters synthesize higher output voltage levels with a better harmonic spectrum and less motor winding insulation stress. Normally the medium voltage drives are available for ratings from 0,4MW to 40MW at the medium voltage level of 2,3kV to 13,8kV as is shown in figure 1.1

For current-source drives, two topologies have found industrial applications in high power ranges: the load-commutated inverter (LCI) and the PWM-CSI. The LCI has been utilized for many years presenting simple converter topology, low manufacturing cost, and reliable operation. Its main problems include low input power factor and distorted input current waveforms, which these problems are overcame by the newer technology of PWM-CSI. Together with the converter topology, great effort has been addressed from the research community in investigating different switching methods for these inverters. This is mainly due to the fact that the adopted switching strategy impacts the harmonic spectrum of output waveforms as well as the switching and the conduction power losses. In case of multilevel converters, three switching methods are usually used.

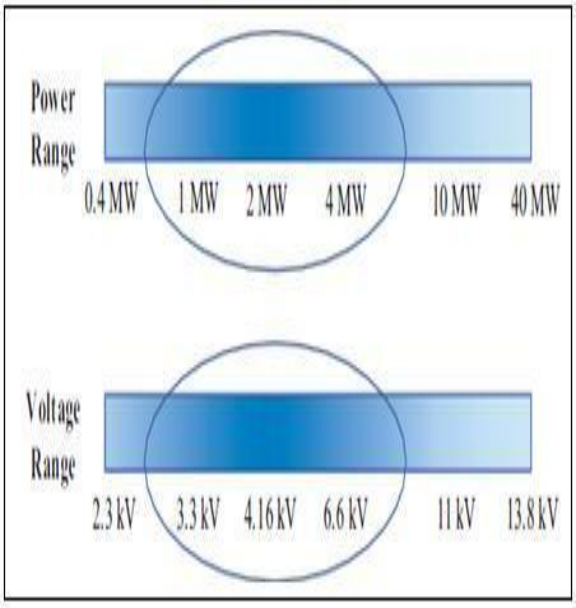

Fig. 1.1: Voltage and Power Range Distribution.

2. Related work

H-bridge multilevel inverter is composed of a multiple units of single phase H-bridge power cells as shown in fig 2.1. These cells are normally connected in cascade on their ac side. In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. This kind of topology requires a number of isolated dc supplies, each of which feeds an H-bridge power cell. The dc supplies are normally obtained from multi pulse diode rectifiers. For the five, seven and nine-level inverters, 12, 18 and 24 pulse diode rectifiers can be employed respectively.

ISSN: 2320-1363

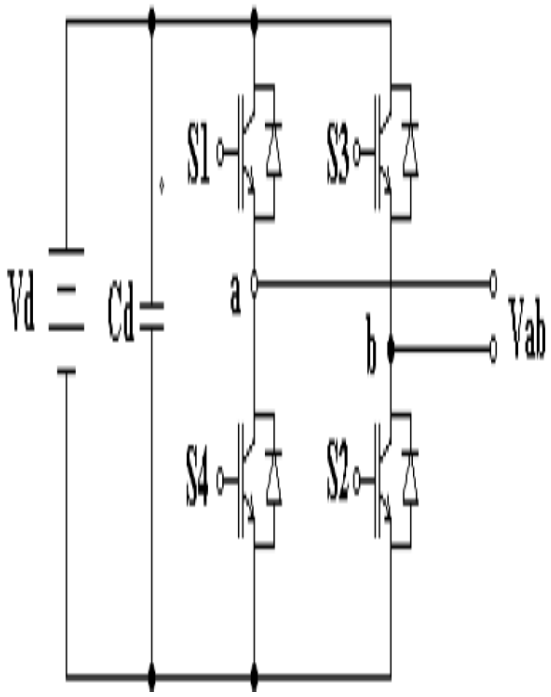

Fig.2.1: Single Phase H- Inverter

Figure 2.1 Single phase H-bridge inverter one of the advantages of this topology is the ability to synthesize higher number of output voltage levels with an excellent harmonic spectrum using low cost and low voltage power semiconductors and capacitors. However, drawbacks of this topology are the large number of power cell devices and of voltages required to supply each cell with a complex and expensive isolated transformer.

The system control strategies, including standalone operation of the new cascade inverter as well as grid-tie operations for different renewable energy sources need to be developed. With the above research motivations, the research objectives can be summarized:

1. To design and build a new cascade inverter that inherits the advantages and overcomes the disadvantages of traditional cascade H-bridge inverters.
2. To solve the zero-crossing distortion problems of single-unit dual-buck inverters.
3. To explore different PWM schemes for further reduction of the switching loss and current ripple.
4. To design and implement standalone controllers for the new cascade inverter.
5. To design and implement grid-tie control of the cascade inverter for different renewable energy and distributed generation sources with the wide-range power flow capability.

3. Methods

In recent years, industry has demanded for high power equipments, which today reaches to megawatts. Adjustable ac drives which operate in high power range are usually connected to the medium voltage network. Hence, medium and high voltage ac drive systems have been considered widely. Today, due to limitation of semiconductor devices to operate in high current and voltage ratings, it is difficult to connect a semiconductor switch directly to medium voltage networks (2.3 – 6.9 kV). To achieve this problem, a family of multilevel inverters has been emerged for working in medium and high voltage levels. Multilevel inverters are power electronic systems that synthesize a desired output voltage from several levels of dc voltages as inputs. In order to do that, multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output

ISSN: 2320-1363

of which generate voltages with stepped waveforms. Some of the most attractive features discussed in the literature reviewed about of multilevel inverters are as follows:

- ✓ They can generate output voltages with extremely low distortion and lower.
- ✓ They draw input current with very low distortion.
- ✓ They can operate with a lower switching frequency.

In this chapter, special attention is focused on the main features of multilevel cascaded H-bridge inverter, different kind of modulation techniques based on carrier based PWM such as: phase-shifted and level-shifted modulations are analyzed and their performance is compared.

3.1 H-bridge Cascaded Topologies

As is known the H-bridge multilevel inverter uses different cells connected in series chain to produce high ac voltage with low distortion currents. The number of cells is chosen typically from 2 to 5, for the worldwide standard machine voltage 2,3kV to 7,2kV. For example for two power cells per phase, the circuit can produce five distinct phase voltage levels. There are several families of H-bridge cells with the same input voltage (460V, 630V and 690V) that are able to produce (800V, 1100V and 1200V) line to line output voltages for rated currents ranging from 70A to 1000A [3]. Nowadays different kind of topologies based on H-bridge cascaded are available in the industry, those, are summarized in table 3.1.1

Drive	Switching Device	Power Range	Manufacturer
Robicon (Perfect Harmony)	1GBT	0.3MVA – 22MVA	Siemens
Tosvert – MV		0.5MVA – 6MVA	Toshiba
Nnovation MV – GP Type H		0.45MVA - 7.5MVA	General Electric

Table 3.1.1: Industrial drives based on H-Bridge multilevel inverters

3.1 H-bridge Cascaded Topologies

As shown in Fig. 2.1, the proposed MLI is composed of two dc-link capacitors (C1, C2) and four switching devices (TA +, TA-, TB +, TB -) comprising an H-bridge, and four active switches (TP +, TP -, TN +, TN -) located between dc-link and H-bridge. The voltage across the switching devices in the dc-link (TP +, TP -, TN +, TN -) is VDC/2 and operated at a switching frequency. Whereas, voltage across the switching devices in the H-bridge (TA +, TA -, TB +, TB -) is VDC and the switches (TA +, TA -, TB +, TB -) are switched at a frequency of the fundamental component of the output voltage (e.g. 50 or 60 Hz). Thus, the dc-link switches (TP +, TP -, TN +, TN -) and the H-bridge switches (TA +, TA -, TB +, TB -) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table I shows the output voltage according to the switching states.

ISSN: 2320-1363

POD-PWM modulation technique for a 5-level inverter

With m_a= 0.79 and m_f=0.34. In this modulation, main harmonics are at the first carrier frequency. In this technique, the odd sidebands around the even carrier multiples, and the even sidebands around the odd carrier harmonics can be easily seen in the output phase voltage spectrum. Also, as with all carrier-based PWM techniques, only the multiples of three away from the carrier multiples cancel in the line spectra; In addition, when this technique is used, an even m_f will lead to both odd and even harmonics in the output phase voltage and in the case of odd m_f, the output phase voltage spectrum will only contain odd harmonics.

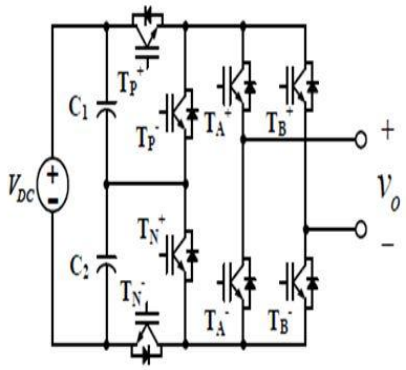

Figure 3.1.2: Proposed Five Level H-Bridge Inverter

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_c \leq V_{ref} < 2V_c$	$V_{dc/2}$ or V_{dc}
Mode 2	$0 \leq V_{ref} < V_c$	0 or V_{dc}
Mode 3	$-V_c \leq V_{ref} < 0$	$-V_{dc/2}$ or 0
Mode 4	$-2V_c \leq V_{ref} < V_c$	$-V_{dc}$ or $-V_{dc/2}$

Table 3.1.3Operating modes and proposed PWM strategy

(POD) Mode 1: A signal subtracted from the reference signal by V_c is compared with the carrier signal. If V-ref $-V_c$> V-carrier, then all switches TP^+ and TN^- are turned on. If V_{-ref} $-V_c$< $V_{-carrier}$, then the switch TP^+ or TN^- is turned off alternately.

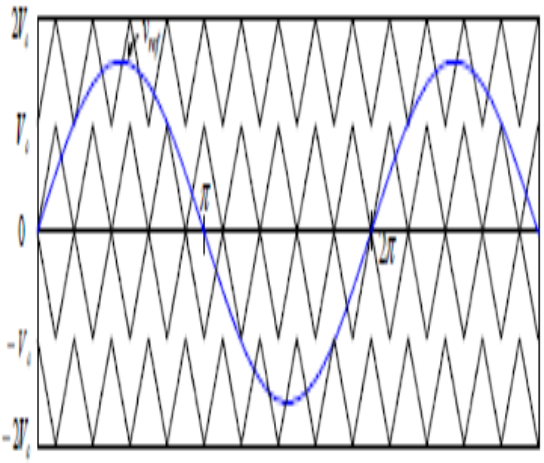

Fig. 3.1.4 Carrier and reference signal arrangements for phase opposition and disposition

Mode 2: The reference signal is directly compared with a carrier signal. If V_{-ref} > $V_{-carrier}$, then the switch TP^+ or TN^- is turned on alternately. If V_{-ref} < $V_{-carrier}$, then all switches TP^+ and TN^- are turned off.

Mode 3: $-V_{-ref}$ is directly compared with a carrier signal. If $-V_{-ref}$ > $V_{-carrier}$, then the switch TP^+ or TN^- is turned on alternately. If $-V_{-ref}$ < $V_{-carrier}$, then all switches TP^+ and TN^- are turned off.

Mode 4: A signal subtracted from $-V_{-ref}$ by V_c is compared with the carrier signal. If $-V_{-ref}$ $-V_c$ > $V_{-carrier}$, then all switches TP^+ and TN^- are turned on. If $-V_{-ref}$ $-V_c$< $V_{-carrier}$, then the switch TP + or TN - is turned off alternately. Only one carrier signal is used to generate eight PWM signals in the proposed PWM method. Thus it is quite simple.

ISSN: 2320-1363

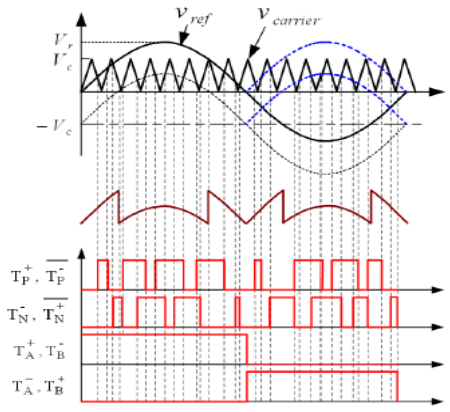

Figure 3.1.5PWM strategy based on POD with carrier signal

Output Voltage (V_o)	Switching Condition			
	T_P^+	T_P^-	T_N^+	T_N^-
V_{DC}	ON	OFF	OFF	ON
$V_{DC}/2$	OFF	ON	OFF	ON
	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF
	OFF	ON	ON	OFF
$-V_{DC}/2$	OFF	ON	OFF	ON
	ON	OFF	ON	OFF
$-V_{DC}$	ON	OFF	OFF	ON

Table 3.1.6 Output voltage according to switching table

Output Voltage (Vo)	Switching Condition	
	TA+,TB-	TA-,TB+
V_{DC}	ON	OFF
$V_{DC}/2$	ON	OFF
	ON	OFF
0	ON	OFF
	OFF	ON
$-V_{DC}/2$	OFF	ON
	OFF	ON
$-V_{DC}$	OFF	ON

Table 3.1.7 Output voltage according to switching table

4. Analysis 2 level inverter (SPWM)

SPWM or sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches. The pulse width modulation inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme SPWM switching technique is commonly used in industrial applications SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of this pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation or SPWM is the mostly used method in motor control and inverter application. In this development a unipolar

ISSN: 2320-1363

and bipolar SPWM voltage modulation type is selected because this method offers the advantage of effectively doubling the switching frequency of the inverter voltage, thus making the output filter smaller, cheaper and easier to implement. Conventionally, to generate this signal, triangle wave as a carrier signal is compared with the sinusoidal wave, whose frequency is the desired frequency, but the two level inverter has the following drawbacks viz,

- Attenuation of the wanted fundamental component of the waveform.
- Drastically increased switching frequencies that leads to greater stresses on associated switching devices and therefore derating of those devices.
- Generation of high-frequency harmonic component

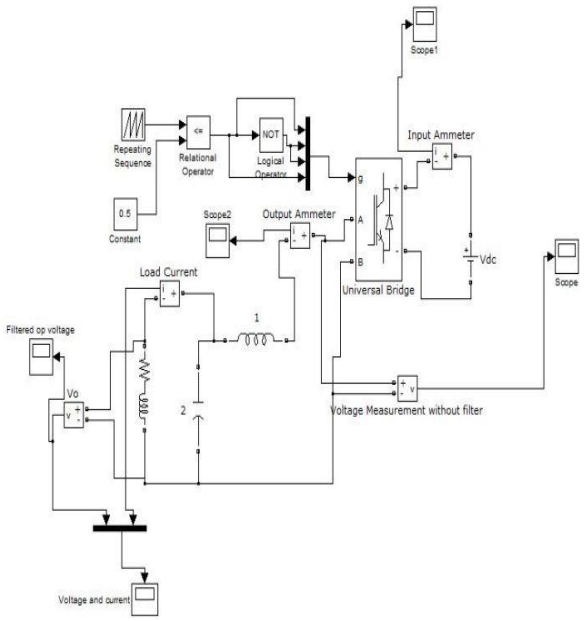

Fig: 4.1 Simulation of a 2 level (SPWM) inverter

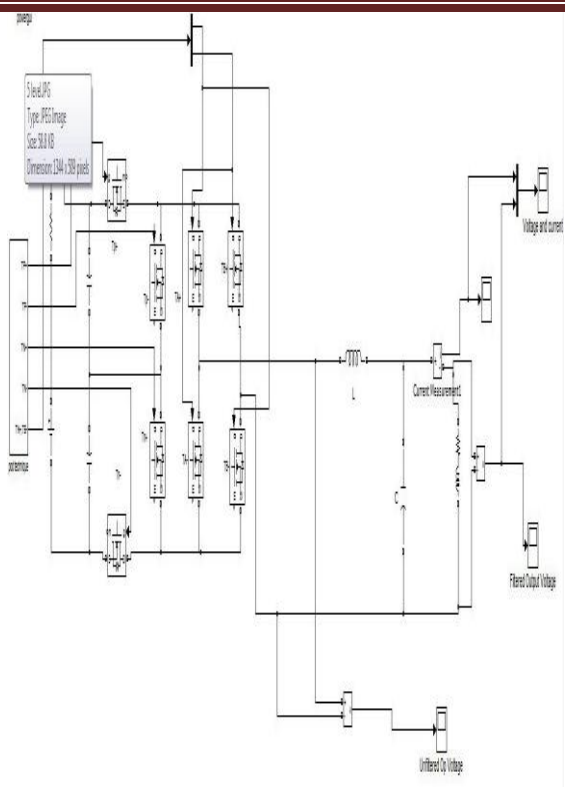

Fig: 4.2 simulation of a 5 level inverter

5. Comparison between Square Wave Operation and Multilevel Inverter

The operating algorithm implemented for inverter operation should mainly concentrate on better efficiency, reduction of parameters like THD in output pole voltages of inverter and thereby improving power factor.

In this perspective POD (phase opposition and deposition) technique has been implemented for a Multilevel Inverter with D.C link switches. Compared to the conventional SPWM techniques used for inverter operation , POD technique when applied to the above stated topology is advantageous since the main H-Bridge switches are switched at fundamental output voltage frequency unlike the in case of SPWM where they are switched at frequency equal to High frequency

ISSN: 2320-1363

triangular wave. There by switching losses in this topology are restricted to minimum possible levels. For the purpose of comparison simulations are carried out for square wave operation where THD will be maximum and switching losses are minimum since the switches are switched at fundamental output voltage frequency.

In order to preserve the switching frequency at the fundamental out voltage frequency and the same time reduce THD.

Two level inverter	Five level inverter
RL-Load (unfiltered)	RL-Load (unfiltered)
THD =48.35%	THD =23.77%
Power factor=0.945	Power factor=0.9522
RL-Load (filtered)	RL-Load (filtered)
THD =8.90%	THD =3.81%
Power factor=0.945	Power factor=0.9956

Table: 5.1 Comparison between 2 level and 5 level inverter

There is not much difference in THD of R-load, RL-load of 2-level inverter and R-load, RL –load of 5-level inverter, because, THD is independent of load. Here the pole voltage is combination of fundamental sine wave and harmonics. By putting a filter at the legs of the inverter and by designing the filter appropriately all the undesirable harmonics in the pole voltage can be filtered out. So by connecting a load after the filter satisfactory performance can be achieved.

6: Simulation and Experimental Results

In this proposed Paper, we have taken various factors to test the simulation coverage.

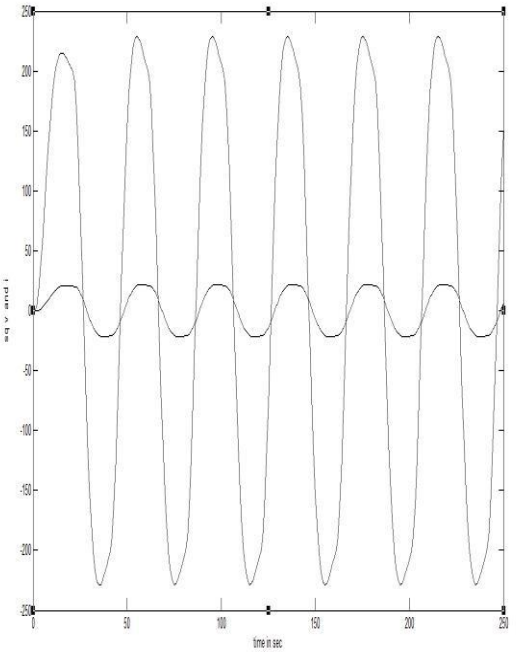

Fig:6.1 Both voltage and current waveforms of 2 level inverter

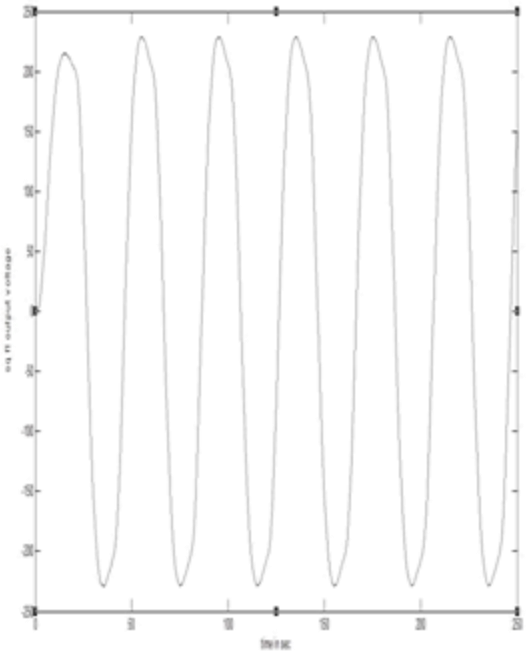

Fig:6.2 Unfiltered 2 level output voltage waveform

ISSN: 2320-1363

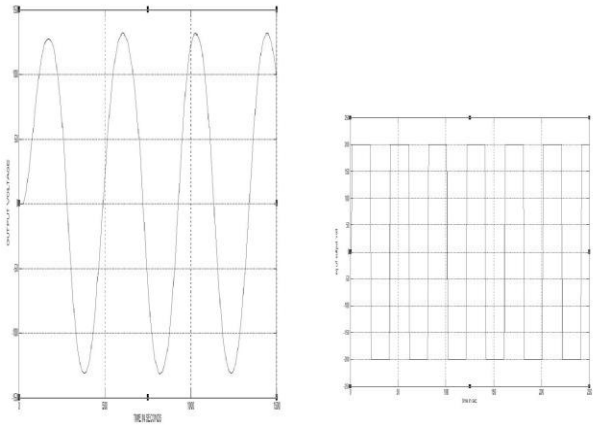

Fig:6.3 filtered 5 level output voltage waveform and unfiltered 2 level output voltage waveform

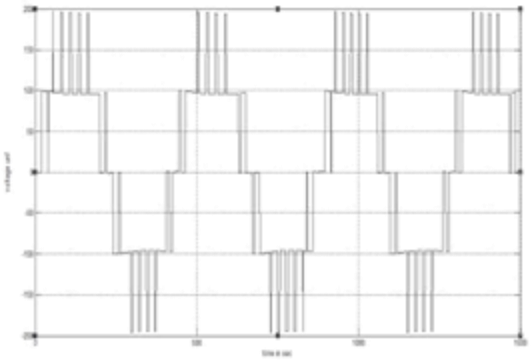

Fig:6.4 Filtered 2 level output voltage waveform

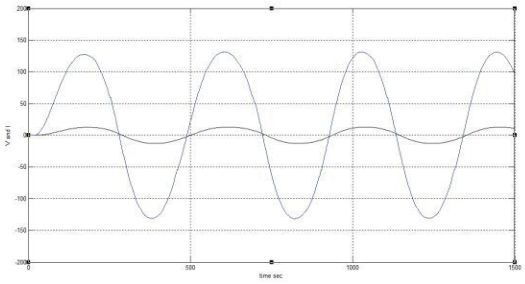

Fig:6.5 Both voltage and current waveforms of 5 level inverter

7. Conclusion

In this paper POD (phase opposition and deposition) technique has been implemented for a Multilevel Inverter with D.C link switches. Compared to the conventional SPWM techniques used for inverter operation , POD technique when applied to the above stated topology is advantageous since the main H-Bridge switches are switched at fundamental output voltage frequency unlike the in case of SPWM where they are switched at frequency equal to High frequency triangular wave. There by switching losses in this topology are restricted to minimum possible levels. For the purpose of comparison simulations are carried out for square wave operation where THD will be maximum and switching losses are minimum since the switches are switched at fundamental output voltage frequency. In order to preserve the switching frequency at the fundamental out voltage frequency and the same time reduce THD. POD technique has been implemented for Single phase 5- Level inverter with D.C link switches and extensive simulations have been carried out in Simulink/Matlab

5. References

[1] H. Abu-Rub, J. Holtz, J. Rodriguez and G. Baoming, "Medium- Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications", IEEE Transactions on Industrial Electronics, Vol. 57, No. 8, pp. 2581-2596, August 2010.

[2] N. A. Rahim, S. Mekhilef, — Implementation of Three - Phase grid

ISSN: 2320-1363

Connected Inverter for Photovoltaic Solar Power Generation System|| Proceedings IEEE. PowerCon 2002. Vol. 1, pp. 570-573., Oct 2002

[3] A. Nabae, I. Takahashi and H. Akagi, —A New Neutral-Point-Clamped PWM Inverter|| IEEE Trans. Ind. Appl., vol. 1A-17, no. 5, pp. 518-523, Sep. 1981.

[4] S.-Y. Park, C.-L. Chen, J.-S. Lai, and S.- R. Moon, —Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter|| , IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1716–1723,Jul. 2008.

[5] E. Villanueva, P. Correa, M. Pacas,—Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems|| , IEEE Trans. Industrial Electronics, Vol. 56, pp. 4399-4406, 2009.

[6] O. Lopez, R. Teodorescu, J. Doval-Gandoy, "Multilevel transformer less topologies for single-phase grid-connected converters" IEEE. IECON 2006, pp. 5191-5196, 2006.

[7] Tae-Jin Kim, Dae-Wook Kang, Yo-Han Lee and Dong-Seok Hyun, —The analysis of conduction and switching losses in multi-level inverter system|| , PESC. 2001 IEEE Vol. 3, pp 1363-1368, 2001.

[7] D.A.B. Zambra, C. Rech, J.R. Pinheiro, "Comparison of Neutral-Point- Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters",IEEE Trans. Ind. Electron., Vol. 57, no. 7, pp2297-2306, July 2010.

[8] M. Calais, "Analysis of multicarrier PWM methods for a single-phase five level inverter", PESC. 2001 IEEE, Vol. 3, pp. 1351-1356, 2001.

[9] B.P. McGrath, —Multicarrier PWM strategies for multilevel inverters|| , IEEE Trans. Ind. Electron., Vol. 49, no. 4, pp. 858-867, 2002.